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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,374	WYNN ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

THIRD DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4,6,8-11,13,15,16,18,19,21,22 rejected under 35 U.S.C. 102(e) as being anticipated by Cepulis et al. (USPN US006463550B1). As appears in claims 1 and 16, Cepulis et al. discloses detecting a memory error in a section of computer memory using a basic input and output system (BIOS); and in response to detecting the memory error, the BIOS instructing an operating system to discontinue use of the section of computer memory with the memory error in column 2, line 55 – column 3, line 26.

3. As per claim 2, Cepulis et al. discloses detecting multiple memory modules in a system; and in response to detecting the multiple memory modules creating a greater number of memory objects to represent respective sections of the multiple memory modules in column 1, lines 28-42; column 3, lines 21-26.

4. As per claim 3, Cepulis et al. discloses creating multiple memory objects to represent respective sections of computer memory; and the operation of instructing the

operating system to discontinue use of the section of computer memory with the memory error comprises sending an eject event from the BIOS to the operating system wherein the eject event identifies the memory object that represents the section of computer memory with the memory error in column 1, lines 28-42; column 3, lines 21-26.

5. As per claim 4, Cepulis et al. discloses receiving the eject event from the BIOS; and in response to receiving the eject event invoking an eject method to disable the section of computer memory with the memory error in column 2, line 55 – column 3, line 26. The eject event will be indicated by the new additional memory device containing the faulty memory location's data and the known map indicating replacement memory locations.

6. As per claims 6 and 21, Cepulis et al. discloses identifying a good subsection and a bad subsection of the section of computer memory with the memory errors; creating a new memory object to represent the good subsection; and instructing the operating system that the new memory object is available for use in column 3, lines 19-26.

7. As per claim 8, Cepulis et al. discloses computer memory; a processor in communication with the computer memory; an operating system residing in the computer memory and executable by the processor; a basic input-output (BIOS) residing in the computer memory executable by the processor, recovery logic in the BIOS that performs operations comprising detecting a memory error in a section of the computer memory; and in response to detecting the memory error instructing the

operating system to discontinue use of computer memory with the memory error in column 1, lines 28-42 and column 2, line 55 – column 3, line 26.

8. As per claim 9, Cepulis et al. discloses the computer memory comprises multiple random access memory (RAM) modules; the information handling system further comprises multiple memory objects that represent respective sections of the multiple RAM modules; and the multiple memory objects are more numbers than the multiple RAM modules in column 2, line 55 – column 3, line 26. The eject event will be indicated by the new additional memory device containing the faulty memory location's data and the known map indicating replacement memory locations.

9. As per claim 10, Cepulis et al. discloses the information handling system further comprises multiple memory objects that represent respective sections of the computer memory; the recovery logic instructs the operating system to discontinue use of the section of computer memory with the memory error by sending an eject event to the operating system; and the eject event identifies the memory object that represents the section of computer memory with the memory error in column 2, line 55 – column 3, line 26. The eject event will be indicated by the new additional memory device containing the faulty memory location's data and the known map indicating replacement memory locations.

10. As per claim 11, Cepulis et al. discloses the operating system receives the eject event from the BIOS; and in response to receiving the eject event the operating system invokes an eject method to disable the section of computer memory with the memory error.

11. As per claim 13, Cepulis et al. discloses identifying a good subsection and a bad subsection of the section of computer memory with the memory errors; creating a new memory object to represent the good subsection; and instructing the operating system that the new memory object is available for use in column 3, lines 19-26.

12. As per claim 15, Cepulis et al. discloses at least first and second nodes, wherein the first node contains the processor and portion of the computer memory, the second node contains another processor and another portion of the computer memory; and wherein, after the recovery logic in the BIOS has instructed the operating system to discontinue use of the section of computer memory with the memory error, the first and second nodes both stop using the section of computer memory with the memory error in column 1, lines 28-42; column 2, line 55 – column 3, line 26.

13. As per claim 18, Cepulis et al. discloses instructions that create multiple memory objects to represent respective sections of computer memory; the instructions to discontinue use of the section of computer memory with the memory comprise an eject event; and the eject event identifies the memory object that represents the section of computer memory with the memory error in column 2, line 55 – column 3, line 26. The eject event will be indicated by the new additional memory device containing the faulty memory location's data and the known map indicating replacement memory locations.

14. As per claim 19, Cepulis et al. discloses an eject method that disables the section of computer memory with the memory error in response to the eject event in column 2, line 55 – column 3, line 26. The eject event will be indicated by the new

additional memory device containing the faulty memory location's data and the known map indicating replacement memory locations.

15. As per claim 22, Cepulis et al. discloses computer memory; at least a first and second processor in communication with the computer memory; a first node comprising the first processor and a first portion of the computer memory; a second node comprising the second processor and a second portion of the computer memory; an operating system residing in the computer memory and executable by the processor; a basic input-output (BIOS) residing in the computer memory executable by the processor; recovery logic in the BIOS that performs operations comprising detecting a memory error in a section of the computer memory; and in response to detecting the memory error instructing the operating system to discontinue use of computer memory with the memory error; and wherein after the recovery logic in the BIOS has instructed the operating system to discontinue use of the section of computer memory with the memory error, the first and second nodes both stop using the section of the computer with the memory error in column 1, lines 28-42; column 2, line 55 – column 3, line 26.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 5,12,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cepulis et al. in view of ACPI Specification 2.0. As per claims 5, Cepulis et al. fails to explicitly state using an advanced configuration and power interface (ACPI) eject control method to disable the section of computer memory with the memory error.

ACPI Specification 2.0 discloses this limitation on page 162, section 6.3.3.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an advanced configuration and power interface (ACPI) eject control method to disable the section of computer memory with the memory error. A person of ordinary skill in the art would have been motivated to use an advanced configuration and power interface (ACPI) eject control method to disable the section of computer memory with the memory error because the ACPI eject command can disable power/data lines of a memory device after the command is invoked. ACPI specification discloses this in section 6.3.3 and on page 252, section 10.12.

18. As per claims 12, Cepulis et al. fails to explicitly state using an advanced configuration and power interface (ACPI) eject control method to disable the section of computer memory with the memory error.

ACPI Specification 2.0 discloses this limitation on page 162, section 6.3.3.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an advanced configuration and power interface (ACPI) eject control method to disable the section of computer memory with the memory error. A person of ordinary skill in the art would have been motivated to use an advanced configuration and power interface (ACPI) eject control method to disable the

section of computer memory with the memory error because the ACPI eject command can disable power/data lines of a memory device after the command is invoked. ACPI specification discloses this in section 6.3.3 and on page 252, section 10.12.

19. As per claim 20, Cepulis et al. fails to explicitly state the eject method comprises an advanced configuration and power interface (ACPI) eject control method.

ACPI Specification 2.0 discloses this limitation on page 162, section 6.3.3.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an advanced configuration and power interface (ACPI) eject control method. A person of ordinary skill in the art would have been motivated to have an advanced configuration and power interface (ACPI) eject control method because the ACPI eject command can disable power/data lines of a memory device after the command is invoked. ACPI specification discloses this in section 6.3.3 and on page 252, section 10.12.

20. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cepulis et al. in view of Jeddeloh (USPN 5974564A). As per claim 7, Cepulis et al. fails to explicitly state wherein the operation of detecting a memory error comprises detecting that an error threshold has been exceeded.

Jeddeloh discloses this limitation in column 6, lines 33-48.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the operation of detecting a memory error comprises detecting that an error threshold has been exceeded. A person of ordinary skill in the art would have been motivated to have the operation of detecting a memory

error comprises detecting that an error threshold has been exceeded because exceeding an error threshold notifies that a serious error is occurring and a component is failing. Jeddeloh discloses this in column 6, lines 33-36.

21. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cepulis et al. in view of Jeddeloh. As per claim 14, Cepulis et al. discloses a memory controller in communication with the processor and the computer memory in column 1, lines 28-42. It is inherent for the memory arrays to have a memory controller.

Cepulis et al. fails to explicitly state a memory address space that the memory controller maps to the computer memory; and wherein the information handling system maps the new memory object available for use by causing the memory controller to add a new range of memory addresses to the memory address space.

Jeddeloh discloses this limitation in column 2, lines 6-25.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a memory address space that the memory controller maps to the computer memory; and wherein the information handling system maps the new memory object available for use by causing the memory controller to add a new range of memory addresses to the memory address space. A person of ordinary skill in the art would have been motivated to have a memory address space that the memory controller maps to the computer memory; and wherein the information handling system maps the new memory object available for use by causing the memory controller to add a new range of memory addresses to the memory address space because adding memory addresses to the memory address space allows for good

memory addresses that have been added to be used instead of bad memory addresses. Jeddeloh discloses this in column 2, lines 20-26.

Response to Arguments

22. Applicant's arguments with respect to claims 1-16,18-22 have been considered but are moot in view of the new ground(s) of rejection. The above disclosed independent claims, except claim 22, have been amended to add a new limitation; therefore the arguments concerning these claims are no longer applicable. The arguments for claim 22 have been found to be persuasive.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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